

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,815,278 B1
DATED : November 9, 2004
INVENTOR(S) : Meikei Jeong et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 11,

Line 54, "the method of claim wherein" should read -- the method of claim 1 wherein --

Column 12,

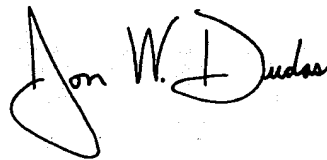
Line 21, "stained" should read -- strained --

Line 30, insert:

-- forming an insulator layer on the structure and bonding the insulator to a handling wafer; selectively removing the carrier wafer, first semiconductor layer and the second semiconductor layer to expose the second graded SiGe alloy; and --

Signed and Sealed this

Fourteenth Day of June, 2005

A handwritten signature in black ink, appearing to read "Jon W. Dudas". The signature is stylized with a large, looped initial "J" and a distinct "D" at the end.

JON W. DUDAS
Director of the United States Patent and Trademark Office